

HIGH PERFORMANCE DIGITAL RADIO CHANNEL SOUNDER FOR USE AT 2 AND 5 GHz

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ABSTRACT

A digital channel sounder has been built to perform measurements of radio channels targeted for 3G and 802.11a operating at 2 and 5 GHz. The novel aspect of the architecture used is that a completely digital wideband modulator and demodulator has been built to allow extensive use of digital signal processing. Such an architecture results in an instrument with significant flexibility, short measurement durations, a rapid update rate and the ability to automatically acquire time and frequency lock.

INTRODUCTION

Future mass-market wireless systems will use higher carrier frequencies, greater on-air bit rates and operate with ever increasing mobility. Accurate models of the dynamic channel amplitude, time and phase characteristics are necessary to aid the design of such systems and products. This paper describes a high performance channel sounder that has been designed and built using high-speed digital signal processing techniques. Such instruments are necessary for the construction of appropriate databases - a prerequisite to production of models.

CHANNEL SOUNDER ARCHITECTURES

Many equipment architectures have been employed for channel sounding over a long period of time. The Cox sliding correlator design Cox [1], Devasirvatham [2] has been used extensively for indoor and outdoor analysis. Such equipment offers excellent dynamic range and good time resolution, but typically has a long measurement period making the architecture less suitable for fast changing environments. Impulse sounders have been used Rappaport [3] offering the advantage of short measurement duration although high RF power is required if significant range is to be achieved.

Recently digital signal processing techniques have been used in a chirp sounder Salous and Gokalp [4] for analysing UMTS channels and a PRBS sounder Kivinen et al [5] for measuring the time varying delay spread between a fixed node and a TGV train entering a tunnel. To date such equipment has typically either used a RAM based data acquisition architecture or pre-sampling analogue compression.

Both techniques give good results but neither offer the combination of continuous, high repetition rate, short

time resolution, long maximum delay-spread and real time results. To achieve these capabilities a sounder has been designed and constructed around a direct digital modulator, high speed intermediate frequency (IF) sampler and FPGA device.

SYSTEM DESIGN

The channel sounder described in this paper is based on a spread spectrum channel sounder architecture whereby a radio frequency carrier is modulated by a high chip rate pseudo-noise (PN) sequence. The inherent processing gain of the spread spectrum waveform allows a long time duration signal to be transmitted with timing resolution proportional to the PN bit rate Grant and Glover [6].

For a typical 'real' channel the signal at the receiver will consist of multiple copies of the transmit waveform, attenuated and delayed in time. At the receiver each discrete signal component is detected by cross-correlation of the received signal with a locally synthesised copy of the PN sequence. Each discrete received signal component yields the transmit signal autocorrelation function.

The radio implementation is a classic double conversion super-heterodyne receiver and a triple conversion super-heterodyne transmitter. Modulation fidelity is maintained at the analogue and digital domain interfaces by the use of direct digital synthesis in the modulator and IF sampling in the receiver.

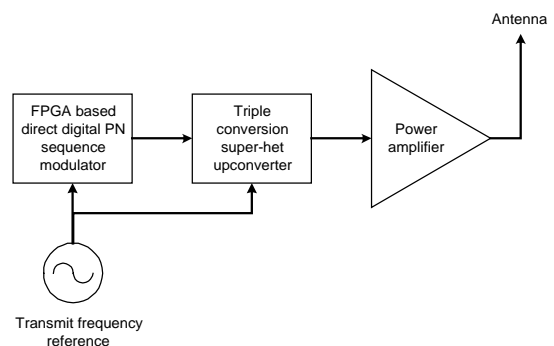


Fig 1. Transmitter architecture.

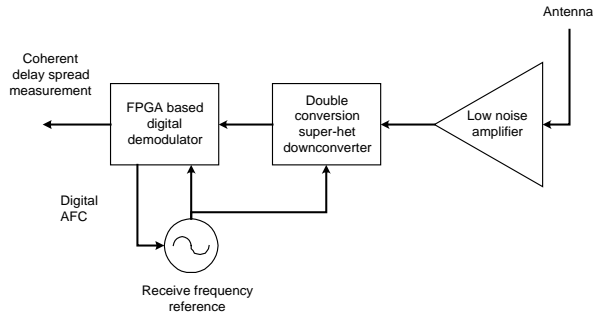


Fig 2. Receiver architecture.

DIGITAL MEASUREMENT TECHNIQUE

The measurement technique implemented involves the generation and transmission of a root raised cosine filtered offset QPSK signal, modulated on each orthogonal component with the same PN sequence offset in time by half the sequence length. A modulation scheme with a return-to-zero (RTZ) format (to ensure a symmetrical symbol shape for each modulated bit) is used to preserve the autocorrelation properties of the PN sequence.

The processing at the receiver end of the channel involves the capture of a burst of signal at least the length of the PN sequence plus the maximum delay spread expected. Following matched root raised cosine filtering the received burst is processed by performing repeated cross-correlation operations between the received signal and a locally synthesised copy of the PN sequence, successively shifted in time by one sample. The received orthogonal components are processed independently and combined to provide a coherent channel sounding impulse response.

Prior to performing the measurement it is necessary to achieve time synchronisation and frequency locking. This is achieved in a phased sequence using a different modulation scheme for each function. The three phases are performed periodically using a frame structure.

Timing Synchronisation. An alternating sequence of 16 bits of data (or dotting) is frequency shift key (FSK) modulated onto the carrier at a low data rate to enable the receive node to acquire time synchronisation with the transmit node. To allow simple detection an FSK tone separation greater than the maximum unlocked frequency error, but low enough to allow considerable decimation prior to detection, is required. The bandwidth reduction inherent in the decimation process increases the received signal-to-noise (S/N) prior to frequency detection, which enables timing synchronisation to be performed at a low carrier-to-noise ratio (C/N).

Frequency Lock. During the measurement it is necessary for the frequency reference in each node to be locked to allow correlation over a significant number of samples. The mobile nature of the measurements and the desire for the measurement equipment not to influence the results precludes the use of a shared frequency source. The chosen solution is to implement

closed loop automatic-frequency-control (AFC) based on an estimate of the frequency offset (δ) calculated at the receiver.

A frequency error between the transmitter and the receiver has two detrimental effects; to reduce the cross-correlation peak amplitude and to potentially introduce increased spurious responses from the orthogonal modulating waveform. Using a worst case approximation the normalised correlation gain can be estimated.

$$g = \sum_{n=-\frac{l-1}{2}}^{\frac{l-1}{2}} \frac{1}{l} \cdot \cos\left(\theta \cdot \frac{n}{l}\right) \quad (1)$$

where l is length of the maximal sequence, θ is the phase shift during the sequence and g is the normalised correlation gain.

Therefore to maintain an output dynamic range of in excess of 35 dB will require a maximum relative phase rotation of less than $\pm 15^\circ$ across the sequence.

Useful results are required with low input C/N in order to maximise the range of the instrument. This requires the transmission of a modulation scheme in the frequency-locking phase that offers additional processing gain but is tolerant to multipath propagation. The scheme adopted is a long CW tone to produce an estimate of frequency error.

QPSK Modulated Maximal Length Sequence. The delay-spread measurement of the channel is based on the transmission of a carrier modulated with a PN sequence with cross-correlation performed at the receiver between a locally synthesised copy sequence and the received signal. The cross-correlation process is run repeatedly using a stored set of received samples with the locally synthesised sequence incrementally offset by one sample each repetition period, i.e.:

$$z_m = \sum_{n=0}^{l-1} rx_n \cdot y_{n+m} \quad (2)$$

where z is the channel sounding results array, rx is the received sample array, y is the locally synthesised PN sequence and l is sample length.

The PN sequence used in a maximal length sequence since it offers the greatest correlation gain and has a constant, low spurious response level.

Offset QPSK modulation has been selected to minimise the modulated signal peak-to-mean ratio thus easing the implementation of the radio hardware. In order to achieve the required modulation fidelity to enable simple correlation logic to be used and also to achieve maximum processing gain, coherent modulation is required.

The same maximal length sequence, offset in time by half the sequence length, is used to modulate both in-

phase and quadrature arms. This is necessary to avoid false correlation peaks that could occur if different sequences were used due to the random phase rotation of the received multipath elements.

The cross-correlation process at the receiver is performed on the output sequence from the matched filter at the sampling rate. The need to constrain the bandwidth of the transmitted signal while ensuring a well-controlled phase trajectory is achieved by implementing root raised cosine matched filtering. The effect of this filtering is to spread the energy into adjacent samples. A unity roll-off factor has been selected as this offers a good compromise between constraining the bandwidth of the emissions and intersymbol interference.

Given the requirement to preserve the autocorrelation properties of the received signal post matched filtering, the raised cosine function of the combined modulation and demodulation filters must result in a return-to-zero symbol. This is achieved by representing the bits of the maximal sequence as either (0, 1, 0, 0) or (0, -1, 0, 0) and using root-raised-cosine filters with a length of two samples.

The effect of this filtering (with unity roll-off factor) can be seen in Table 1 using an example of a 7-bit maximal length sequence.

Sequence
Maximal sequence
0,0,1,1,1,0,1
Modulator input impulse sequence with nulls
0,-1,0,0,0,-1,0,0,0,1,0,0,0,1,0,0,0,-1,0,0,0,1,0,0
Output sample sequence at receiver
0,-1/2,-1,-1/2,0,-1/2,-1,-1/2,0,1/2,1,1/2,0,1/2,1,1/2,0,1/2,1,1/2,0,-1/2,-1,-1/2,0,1/2,1,1/2,0

Table 1 Modulated signal maximal properties.

MEASUREMENT CAPABILITY

The measurement capability of the sounder is primarily determined by the sequence length, sample rate of the converters used and the transmit power.

With the same maximal length sequence used on each orthogonal arm (offset by half a sequence length), the maximum delay spread measurable without ambiguity is half the code length. The time domain resolution of the correlation output will be of the order of the converter sampling rate and the channel range will be determined by the processing gain of the PN sequence and the transmit power.

The equipment has been designed and built primarily to support investigations of mobile and indoor/outdoor interface channels. The architecture and implementation described in this paper has produced an instrument with the following capabilities.

Time domain resolution: 10 ns, maximum delay spread: 10 μs, range: 2 km measurement repetition rate: 5 ms and minimum usable input C/N: 0 dB

DIGITAL IMPLEMENTATION

The architecture and implementation of the digital-signal-processing is based around high-speed converters operating at 180 Msamples/s in the receiver and transmitter with logic processing functions performed in a Field Programmable Gate Array.

Maximal sequence length. A sequence of twice the length of the maximum delay spread is required. With four complex samples per sequence bit and a required sequence length of in excess of 20 μs a 511-bit maximal length sequence has been used.

Modulator. The transmitted waveform is generated using direct digital synthesis. A digital-to-analogue converter with a sampling rate (f_s) of 180 Msamples/s driven by a digital modulator generates a modulated intermediate frequency at $1/4 f_s$. The use of a direct digitally synthesised modulated transmit IF ensures the generation of accurate quadrature components with correct modulation shaping without the need for calibration. The baseband constellation diagram is shown in Figure 3.

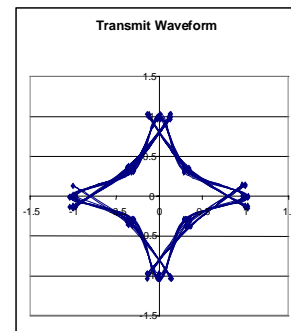


Figure 3. Modulation constellation.

Receiver Sampling and Down-Conversion. To ensure modulation fidelity is preserved at the receiver intermediate frequency sampling is performed. To allow a higher frequency final analogue IF the wanted signal is sampled at $3/4 f_s$.

Digital down-conversion to baseband is performed by multiplying the input sample sequence by orthogonally phased oscillators, i.e.:

$$f_{loI} = \sin\left(\frac{2\pi f_s}{4}\right) f_{loQ} = \cos\left(\frac{2\pi f_s}{4}\right) \quad 3(a \& b))$$

Given that the frequency of the local oscillators are $1/4 f_s$, down-conversion of I and Q channels can be implemented efficiently by repeatedly multiplying the input samples by 0,1,0,-1 and 1,0,-1,0 respectively. This avoids the need for fast multipliers. The resultant I and Q value pairs (forming a single complex sample) are however offset in time due to the use of alternate samples for each in the down-conversion process. Realignment in time can be performed simply in the receive FIR filter.

Timing Recovery. Implementation of the timing acquisition function is based on the transmission of 16 bits of dotting, each bit comprising 2^{14} complex samples (182 μ s) with four periods of FSK modulation (approximately 22 kHz). Decimation by 128 complex samples is performed followed by a test to determine if there has been a net phase advance or retardation between adjacent decimated samples. Integration of the results of 32 successive phase rotation tests, gives four quantitative estimates of the phase rotation direction per dotting bit period. The estimates of phase rotation are then compared against separate positive and negative thresholds to yield a sequence of 64 positive deviation, negative deviation or indeterminate results. From this sequence time synchronisation can be achieved under multipath conditions and at 0 dB C/N.

Frequency Lock. With a carrier frequency of 5.225 GHz and a maximal length sequence of 511 bits transmitted over a period of 20 μ s it can be shown (1) that a maximum phase shift of $\pm 15^\circ$ is acceptable across the sequence. This requires a relative frequency error of less than ± 0.8 ppm. Performance considerably better than this should be possible given the bandwidth of the channel and high sampling rates.

The implementation of the frequency locking function is based on the transmission of a CW tone. As with the time synchronisation process decimation is performed over 128 consecutive complex samples to allow frequency error estimates to be performed at poor input C/N. The phase difference between adjacent decimated outputs is then determined. Integration of 256 successive phase difference results provides further noise suppression with the final frequency error estimate being equivalent to averaging over 32767 complex samples.

Correlation. With the input sequence held in a 4×511 word long shift register and the locally synthesised sequence represented as 1 or -1, addition and subtraction can be used instead of multiplication to reduce the required processing power. Additionally the orthogonal received components are processed sequentially with each cross-correlation calculated in four clock cycles to further reduce processing load. The result is a system capable of performing 2044 complex correlations on 511 words of data in less than 200 μ s. The results from a logical simulation of the correlation algorithms used is shown in figure 4. with an input C/N of 3 dB.

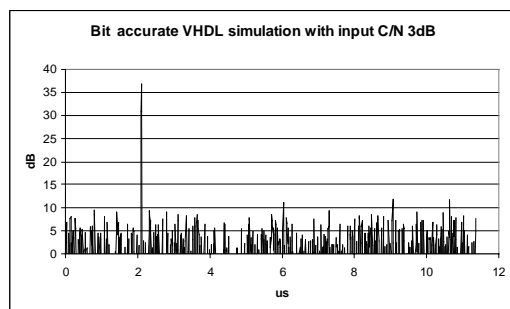


Figure 4. Channel sounding simulation result.

CONCLUSIONS

A cross-correlation based channel sounder for the 2 and 5 GHz frequency bands has been presented. Its structure and digital implementation gives it the ability to perform multiple incrementally offset cross-correlations with the same set of stored input samples. The result is a significantly reduced measurement time when compared to sounders based on traditional analogue techniques. A realisation based around a high-speed FPGA device results in a fast repetition rate enabling the measurement of rapidly changing channel characteristics with near real-time results.

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